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REMARKS

The claims are revised in response to the objections and rejections in the Office action identified above. Claims 1-12 remain, with no claim previously allowed.

A new Title is submitted in response to the Examiner's statement that the original title is not descriptive.

The objections to certain claims are noted. Responding to those objections, Claims 2 and 4 are revised to remove the parentheses around the equations. Those claims are also revised, and Claim 12 is revised, by adding --that obeys the equation--, as suggested by the Examiner. The amended claims are submitted as being free of the grounds for objection noted by the Examiner in the last Office action.

Turning to substantive issues, Claims 1-9 and 12 are rejected as unpatentable over *Hill* (US 6,028,348) in view of newly-cited *Sovero* (US 5,378,922). The Applicant respectfully traverses this rejection.

Regarding *Hill*, the Applicant repeats and incorporates by reference the remarks with respect to that reference in the Second Response filed May 22, 2006.

Turning to *Sovero*, that reference discloses an integrated structure with a transistor and a semiconductor resistor. The semiconductor resistor is formed in the subcollector layer of the transistor. As shown in Fig. 2 and described in column 3, lines 32-37 of *Sovero*, contact layers are deposited on the emitter, the collector, and the base of the transistor. Moreover, by way of a conductor deposited and patterned on the integrated structure, an ohmic connection is formed between the emitter of the transistor and the semiconductor resistor.

As can be seen from the cross-sectional views of the structure in Figs. and 3 and 4 of *Sovero*, the conductor connecting the emitter and the resistor has to pass over the layers between the emitter and the subcollector, namely, the base and collector layers. (The schematic representation for that connection of the resistor 16 is seen in Fig. 1.) In order to avoid short-circuiting these layers, there must be a passivating layer present between the conductor and the underlying structure. A passivation layer is not explicitly mentioned in *Sovero*; however, such a layer must be present to ensure the integrity of the device, as is known to those skilled in the art. The absence of its mention in *Sovero* is likely for the purpose of simplifying the description in that document.

(Concerning passivation layers generally, the undersigned refers to US Patents 7,098,545; 7,095,105; and 7,093,356.)

In contrast with *Sovero*, in the structure of the present invention a passivation layer underneath the metallization layer which is formed as a lower one of the wiring levels is omitted. This follows from Fig. 1 and page 4, lines 4-12 of the present application, stating that the lower wiring level 30 comprising the metal contact 4 and the metal sections 5, 6 is on top of the subcollector layer 3. As further described at page 4, lines 15-27, a passivation layer 8 is deposited above a lower wiring level 30.

To distinguish the present invention over the art including *Sovero*, the Applicant is amending Claim 1 to state that the lower one of the wiring levels is deposited directly on top of a subcollector layer without a passivation layer underneath the lower wiring level. That lower one of the wiring levels connects the at least one active component with at least one passive component, in the integrated circuit arrangement of amended Claim 1. This feature has the advantage that there are fewer processing steps necessary

in order to form the lower wiring level. Furthermore, due to the absence of a passivation layer underneath the wiring level, the occurrence of stray capacitances is minimized. The combination of that claim thus defines over *Sovero* as possibly combined with *Hill*, and nothing in either reference would have led one of ordinary skill to produce the arrangement as now defined by Claim 1. Accordingly, Claim 1 and the claims depending therefrom are patentable over *Hill* in view of *Sovero*.

Claim 10 is rejected as unpatentable over *Hill* in view of *Sovero*, and further in view of *Baba* (US 6,853,054). The Applicant respectfully traverses that rejection for the reasons given above with respect to *Hill* and *Sovero*. Regarding *Baba*, that reference is cited as disclosing a micro-strip conductor formed by means of various wiring levels in a semiconductor device. However, nothing in that reference discloses or suggests that novel and unobvious combination of structural elements recited in parent Claim 1. For that further reason, Claim 10 is patentable over the applied art.

Claim 11 is rejected as unpatentable over *Hill* in view of *Sovero*, further in view of *Shimamoto* (US 6,683,260). *Shimamoto* is cited as disclosing a waveguide in a multilayer wiring board. However, that reference and the other two references fail to disclose or teach an integrated circuit arrangement having the novel combination of elements in Claim 11 including its parentage. Accordingly, Claim 11 would not have been obvious to one of ordinary skill in view of the applied art.

Claims 2, 4-8, and 12 are rejected under the alternate grounds of being unpatentable over *Hill* in view of *Sovero* as applied to Claim 1, further in view of *Ko* (US 6,696,538). This alternate rejection was presented in the event —now effective, due to the present amendments of Claims 2 and 4— that the recitations enclosed in

parentheses (Claims 2 and 4) are considered as having an effect on the scope of the claims. The Applicant respectfully traverses that alternate ground of rejection, for the reasons mentioned above with regard to Claim 1. *Ko* is cited as teaching a small dielectric constant below 3, but nothing in that reference (taken along with *Hill* and *Sovero*) suggests the limitations of the claims including parent Claim 1. Accordingly, Claims 2, 4-8 and 12 define patentable subject matter over the applied art.

Claim 11 is rejected on the alternate ground of *Hill* in view of *Sovero* and *Ko*, further in view of *Baba*. Claim 11 is rejected on the alternate ground of being unpatentable over *Hill* in view of *Sovero* and *Ko*, further in view of *Shimamoto*. The Applicant respectfully traverses both rejections. The references, singly or in the applied combinations, would not have disclosed or suggested the claimed structure to one of ordinary skill.

The foregoing is submitted as a complete response to the Office action identified above. The Applicant respectfully submits that all claims now in this application are patentable over the art of record and solicits a notice of allowance.

Respectfully submitted,

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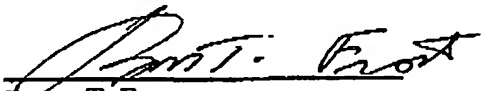

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